REMARKS

Examiner Rajnikant B. Patel is thanked for the thorough examination and search of the subject Patent Application.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection of claims 1-13, and 16-23 under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 2 and Jeon et al (U.S. patent # 6,222,412 B1) is requested, based on the following remarks:

Jeon et al. disclose (col. 1 lines 6-13) :

> "The present invention relates to a circuit for controlling waveform distortion at a control terminal of high frequency transistor, more specifically, to a circuit for controlling waveform distortion resulting from nonlinearity of the impedance of a control terminal (gate or base) capacitance of a transistor, which can be employed in circuits showing a nonlinearity performance of high frequency amplifier or oscillator."

The claimed invention teaches:

> "This invention relates generally to voltage regulators, and more particularly to an enhancement of low dropout voltage regulators having an adaptive biased driving stage in order to improve stability through a very wide range of output current."

Jeon et al. teach a topic very different to the topic of the claimed and it is believed to be non-obvious to use an impedance to control waveform distortions at a

control terminal of a high frequency transistor with the claimed invention namely a pass transistor of a low drop-out regulator.

It is even more non-obvious because Jeon suggests in Fig. 4(A) the usage of a shunt capacitor between the gate terminal and source terminal of a FET. Jeon et al teach (col.2, lines 28-35):

> "In this connection, a method for controlling the distortion of the sine wave by regulating the ratio of the gate capacitance in a range of above and below Vp viewed from the X side of FIG. 2 to have a value of approximately 1, has been suggested in the art. This method was realized by **employing a shunt capacitor**(Cs) between the gate terminal and source terminal of FET as in **FIG. 4(A)** (see: Paul M. White, IEEE MTTs, pp.277-280(1994)). This circuit, as can be seen in FIG. 4(B), has its merits of relaxing the nonlinearity of the gate capacitance by increasing the capacitance at the input terminal of FET to the level of Cs."

A combination of prior art as shown in applicant's Fig. 2 with a shunt capacitor as shown in Jeon et al.'s Fig. 4a would not work for an LDO of the claimed invention.

Furthermore Jeon et al. does not suggest to use the impedance shown in their Fig. 4(A) for applications as e.g. an LDO of the claimed invention. Therefore a modification of applicant's prior art by utilizing the technique taught by Jeon et al. is believed to be non-obvious and wouldn't work properly.

The claimed invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination of these two references cannot be made

without reference to Applicant's own invention. The processes of claims 1-13 and claims 16-23 are both believed to be novel and patentable over these various references because there is not sufficient basis for concluding that the combination of the claimed elements would have been obvious to one skilled in art. That is to say that something in the teaching of Jeon et al. or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request examiner Rajnikant B. Patel to reconsider his rejection in view of these arguments.

Reconsideration of the objection to claims 14-15 as being dependent upon a rejected base claim, but being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim is requested, based on the following remarks:

Claims 14-15 are dependent claims upon base claim 1 which is believed to be patentable according the arguments above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 845-452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761